REMARKS

This is a response to the Office action mailed November 20, 2007. For this response, 19 claims remain pending in the application. Claims 1, 9 and 15 were cancelled by a previously filed amendment. Claims 4, 11 and 17 are amended by the amendment being submitted herewith. Claims 2 – 8, 10 – 14, and 16 – 22 stand rejected. The Applicants respectfully traverse the rejections and request reconsideration.

Rejection Of Claims 4, 11 and 17 Under 35 U.S.C. §112, First Paragraph

The Examiner has rejected claims 4, 11 and 17 under 35 U.S.C. §112, first paragraph, on grounds that they recite subject matter not described in the specification. In particular, the Examiner states that these claims recite that the interconnection substrate includes "only a conductive interconnection layer", and that this language is not supported by the specification. The Applicants respectfully disagree.

Throughout the specification, the interconnection substrate is described as including an interconnection layer having the purpose of distributing power and ground throughout the semiconductor substrate. While the Applicants agree that the interconnection substrate may include other elements and that it may perform additional purposes, the Applicants respectfully submit that the specification is clearly supportive of an interconnection substrate that only includes a conductive interconnection layer that performs only the purpose of distributing ground and power to the semiconductor substrate. Just because the interconnection substrate may include additional elements and perform additional functions, this does not mean that the interconnection substrate cannot be limited to performing only its primary function of distributing power and ground to the semiconductor substrate and consisting only of elements necessary to carry out that primary function.

Nevertheless, claims 4, 11 and 17 have been amended by the amendment being filed herewith to remove the language objected to by the Examiner. Therefore, this rejection is believed to be moot, and the Applicants respectfully request that it be withdrawn.

Rejection of Claims 20 – 22 under 35 U.S.C. §102(a)

The Examiner has rejected claims 20 – 22 under 35 U.S.C. 102(a) as being anticipated by Farook, et al. The Applicants respectfully traverse the rejection for at least the following reasons.

The Examiner has construed the passive components 10 described in Farook, et al. as being the same as the interconnection substrate of the invention recited in claims 20 – 22. The Applicants respectfully disagree with the Examiner's construction of this claim element. The passive components 10 described in Farook, et al. are not substrates, but are individual passive components (resistors, capacitors, filters, indictors, etc.) formed in cavities 30 in the substrate 50. These components perform the corresponding electrical and/or magnetic functions normally associated with them. Thus, their primary purposes are to perform their respective functions. By placing them in cavities and electrically connecting them via pads 42, the lead lengths normally associated with connecting these types of passive components in an IC package are shortened, which reduces noise in the IC package and improves the effectiveness of the passive components. The passive components 10 are not "substrates", but rather, are discrete components located in cavities 30 formed in the substrate 50. For at least this reason, the Applicants respectfully submit that the rejection is improper and request that it be withdrawn.

In addition, although the passive components 10 couple electrical charge between the semiconductor device 20 and the substrate 50, their primary functions are not to distribute power and ground. As stated above, the primary functions of the interconnection substrate of the invention is to distribute power and ground to the semiconductor device and to provide electrical pathways between the power supply and ground connections of the substrate 12 and the conductors and integrated circuit of the substrate 14. Therefore, the Examiner's finding that the passive components 10 of Farook, et al. are "operable to receive power directly from a third substrate and distribute the power to the semiconductor substrate, the interconnection substrate having a surface area smaller than the semiconductor substrate surface area", as recited in independent claim 20, is incorrect. For at least this additional reason, the Applicants respectfully submit that the rejection is improper and request that it be withdrawn.

Rejection Of Claims 2 – 5, 7, 8, 10, 11, 13, 13, and 16 - 18 Under 35 U.S.C. §103(a)

The Examiner has not rejected independent claim 4 under 35 U.S.C. §102 or 35 U.S.C. §103. Therefore, the Applicants respectfully submit that the rejection of claims 2 – 5, 7, and 8, all of which depend either directly or indirectly from claim 4, under 35 U.S.C. §103(a) as being unpatentable over Degani, et al. in view of Ishikura, is improper. The dependent claims cannot be rejected under 35 U.S.C. §103 without first rejecting the claim from which they depend under 35 U.S.C. §102 and/or 103. Accordingly, the Applicants respectfully submit that the rejection of claims 2 – 5, 7, and 8 is improper and request that it be withdrawn. Nevertheless, the patentability of independent claims 4, 11 and 17 over Degani, et al. in view of Ishikura will be explained below in detail.

As will now be described, for at least the reason that the neither of the chips 19 and 20 shown in FIGs. 1- 8 of Degani, et al. is an “interconnection substrate”, as recited in independent claims 4, 11 and 17 of the present application, the rejection is improper, and the Applicants respectfully request that it be withdrawn.

As stated in the previous response filed by the Applicants on September 18, 2006, the elements 19 and 20 shown and described in Degani, et al. are silicon chips that are bonded to a silicon substrate 18. It is well know in the art that a “chip” includes a semiconductor component. Thus, chips 19 and 20 include a semiconductor component. Therefore, the chips 19 and 20 are analogous to, for example, the semiconductor substrate 14 of the invention, not the interconnection substrate 16 of the invention (FIG. 1). Consequently, the silicon substrate 18 is analogous to the interconnection substrate 16 of the invention, not the semiconductor substrate 14 of the invention. Therefore, unlike the interconnection substrate 16 of the invention, the surface area of Degani, et al.’s silicon substrate 18 is larger than the surface area of Degani, et al.’s chip 19, or the surface area of Degani, et al.’s chip 20. Each of in independent claims 4, 11 and 17 of the present application recites that the surface area of the semiconductor substrate is larger than the surface area of the interconnection substrate, which is the opposite of what is taught in Degani, et al.

The Examiner states that Degani, et al. fails to disclose a semiconductor substrate including a circuit and relies on Ishikura as teaching a semiconductor substrate including an integrated circuit. The Examiner then concludes that it would have been obvious to incorporate the semiconductor substrate including the circuit of Ishikura into the ICP disclosed in Degani, et al. As described above, this reasoning is flawed because Degani, et al. does indeed teach a semiconductor substrate including a circuit being included in the ICP, namely, chips 19 and 20. The meaning of “chip” is also clearly set forth in the Background of Degani, et al. in Column 1, lines 36 – 37:

“[t]he integrated circuit unit may include a semiconductor chip (a die), or multiple semiconductor chips….” The Applicants respectfully submit that the Examiner appears to be ignoring this plain meaning of the term “chip”. Also, if the silicon substrate 18 is replaced with one of the semiconductor substrates disclosed in Ishikura, then there would be no substrate for the dies 19 and 20, which would render the ICP of Degani, et al. inoperable.

For at least these reasons, the Applicants respectfully submit that the rejection of independent claims 4, 11 and 17 is improper and request that it be withdrawn. Because each of the dependent claims 2 – 5, 7, 8, 10, 13, 14, 16 and 18 depend directly or indirectly from one of independent claims 4, 11 and 17, these dependent claims are also patentable over Degani, et al. in view of Ishikura, and the Applicants respectfully request that the rejection of these claims also be withdrawn.

Rejection Of Claims 6, 12 and 19 Under 35 U.S.C. §103(a)

Claims 6, 12 and 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Degani, et al. in view of Ishikura and further in view of Kelly, et al. The Applicants respectfully traverse this rejection. Nevertheless, for at least the reason that dependent claims 6, 12 and 19 depend directly or indirectly from one of these independent claims, these claims are also patentable over Degani, et al. in view of Ishikura and further in view of Kelly, et al. Therefore, the merits of this rejection will not be addressed since these claims are allowable for at least the reasons described above with reference to the independent claims. Accordingly, the Applicants respectfully request that the rejection of these claims also be withdrawn.

Conclusion

For the reasons set forth above, it is respectfully submitted that all pending claims are in condition for allowance. Applicants respectfully request reconsideration of the rejections and allowance of the application. Should there be any further questions or concerns, the Examiner is urged to telephone the undersigned to expedite prosecution.

Respectfully submitted,
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